FIG. 1
(PRIOR ART)

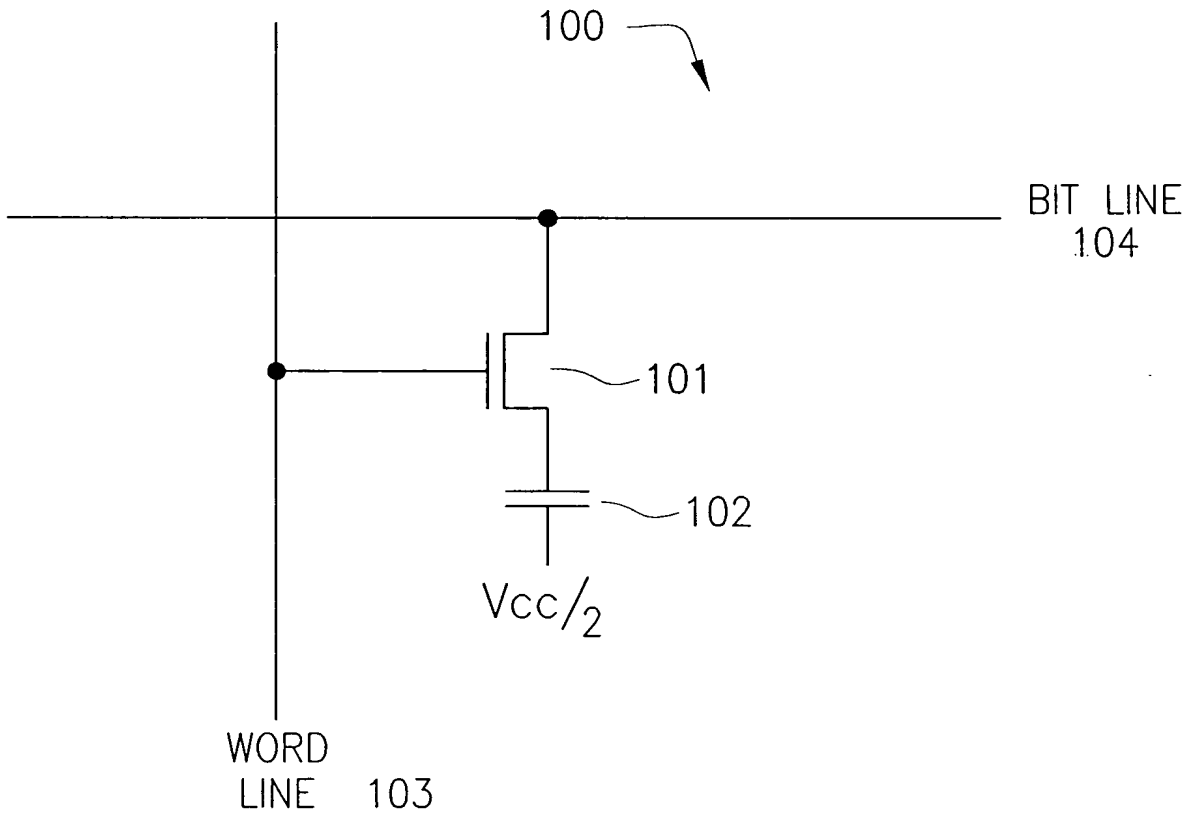


FIG. 2
(PRIOR ART)

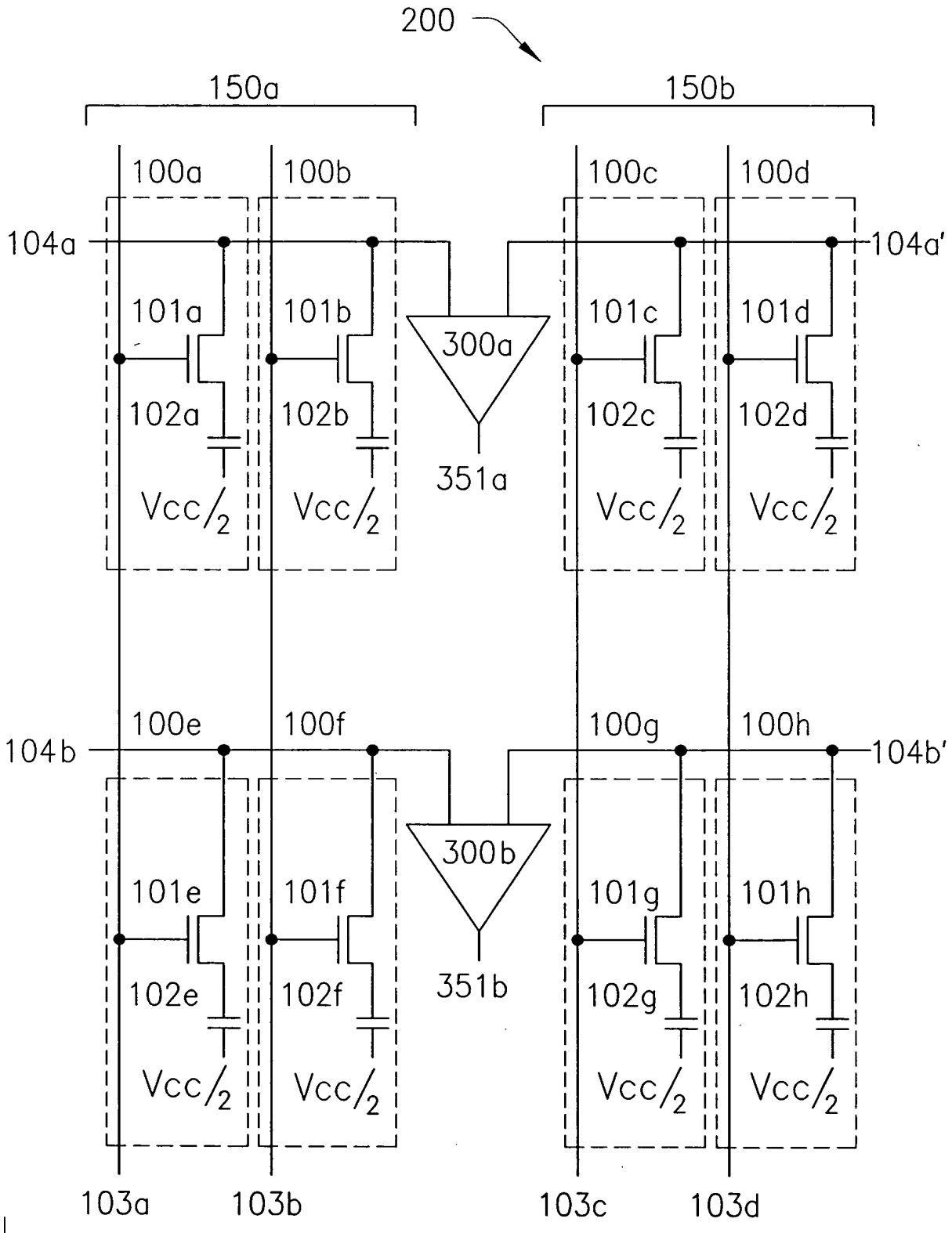


FIG. 3
(PRIOR ART)

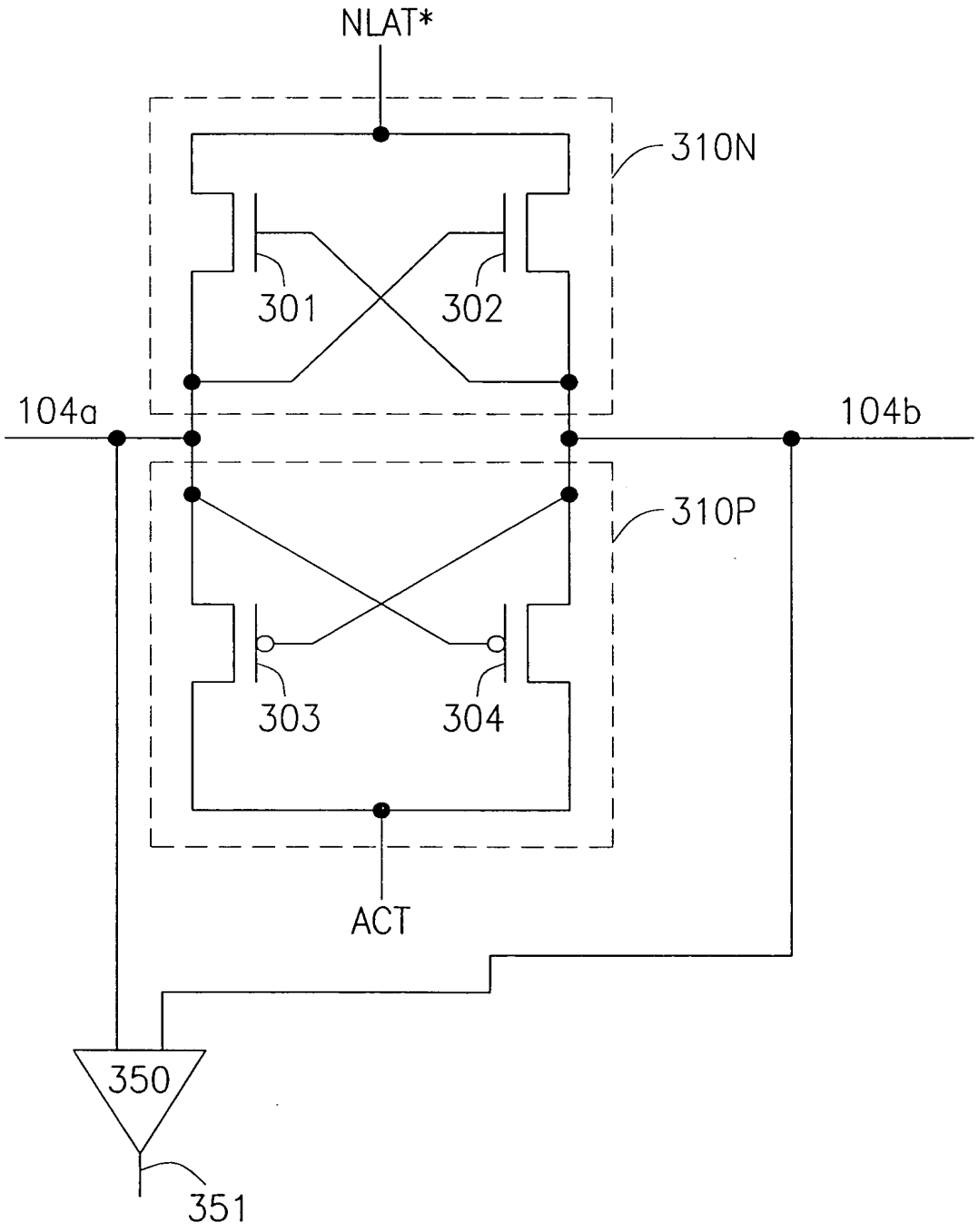


FIG. 4

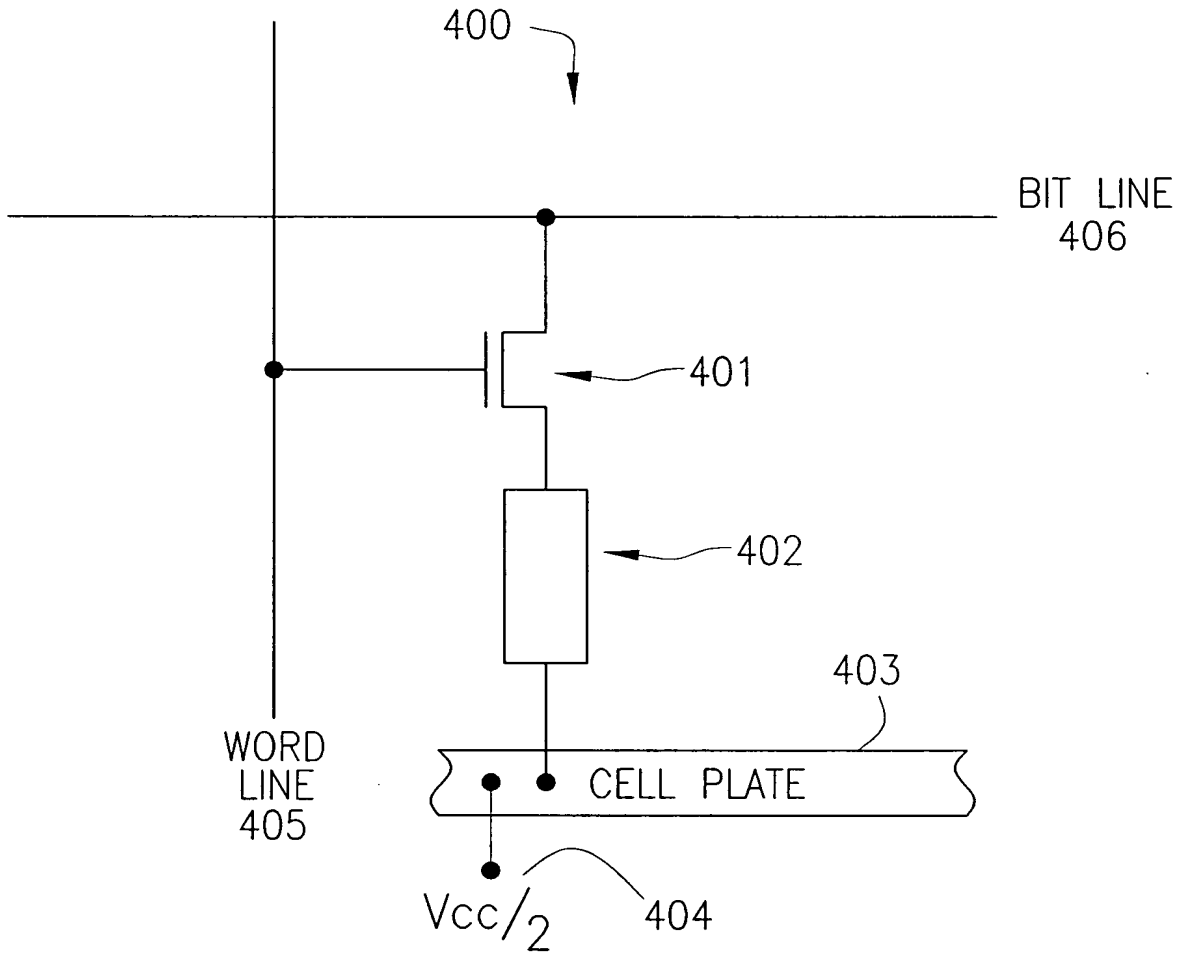


FIG. 5

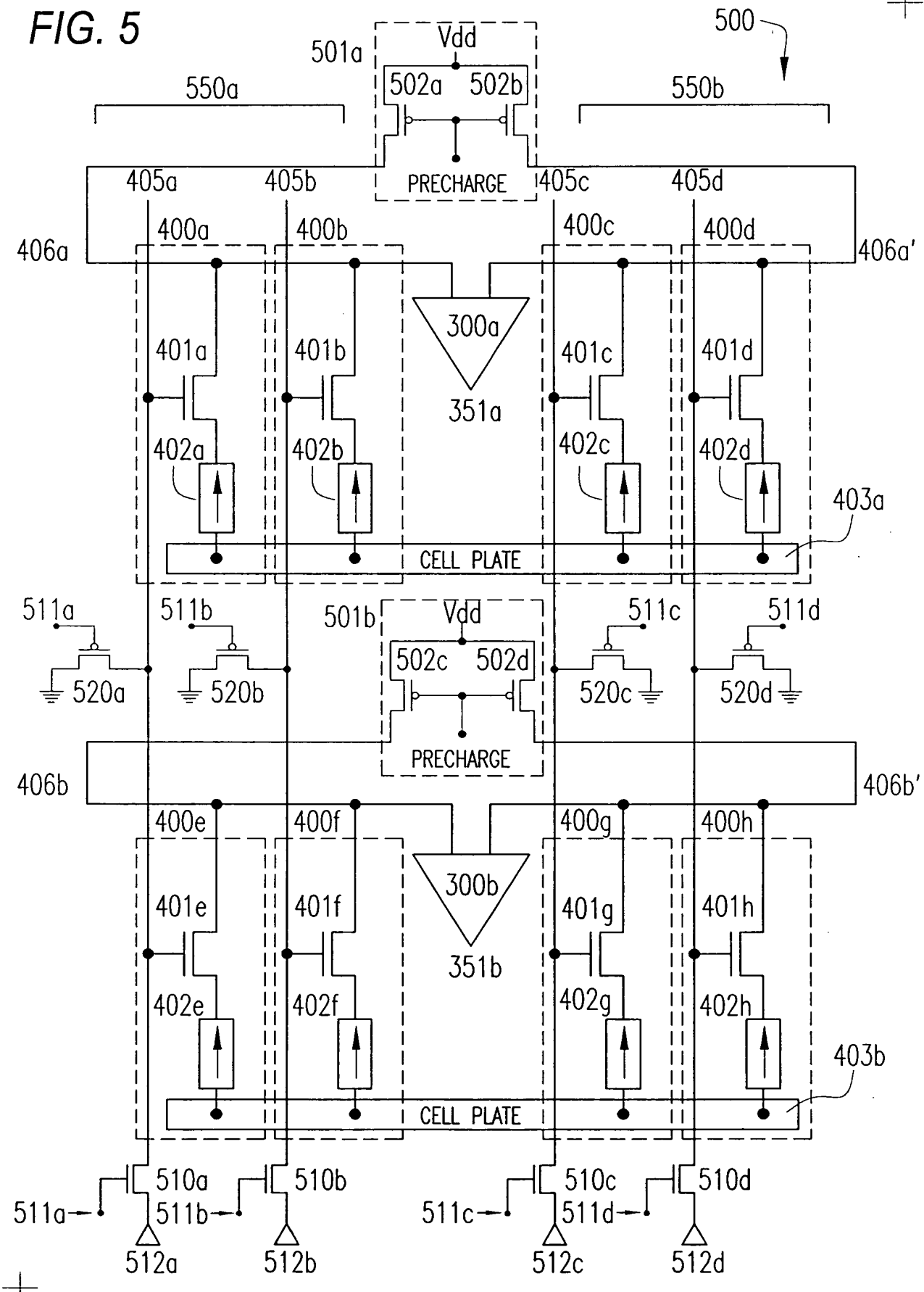

500
501a
Vdd
502a
502b
PRECHARGE
550a
550b
405a
405b
405c
405d
406a
406a'
400a
400b
400c
400d
300a
351a
401a
401b
401c
401d
402a
402b
402c
402d
403a
CELL PLATE
511a
511b
511c
511d
501b
Vdd
502c
502d
520a
520b
520c
520d
PRECHARGE
406b
406b'
400e
400f
400g
400h
300b
351b
401e
401f
401g
401h
402e
402f
402g
402h
403b
CELL PLATE
510a
510b
510c
510d
511a
511b
511c
511d
512a
512b
512c
512d

FIG. 6A

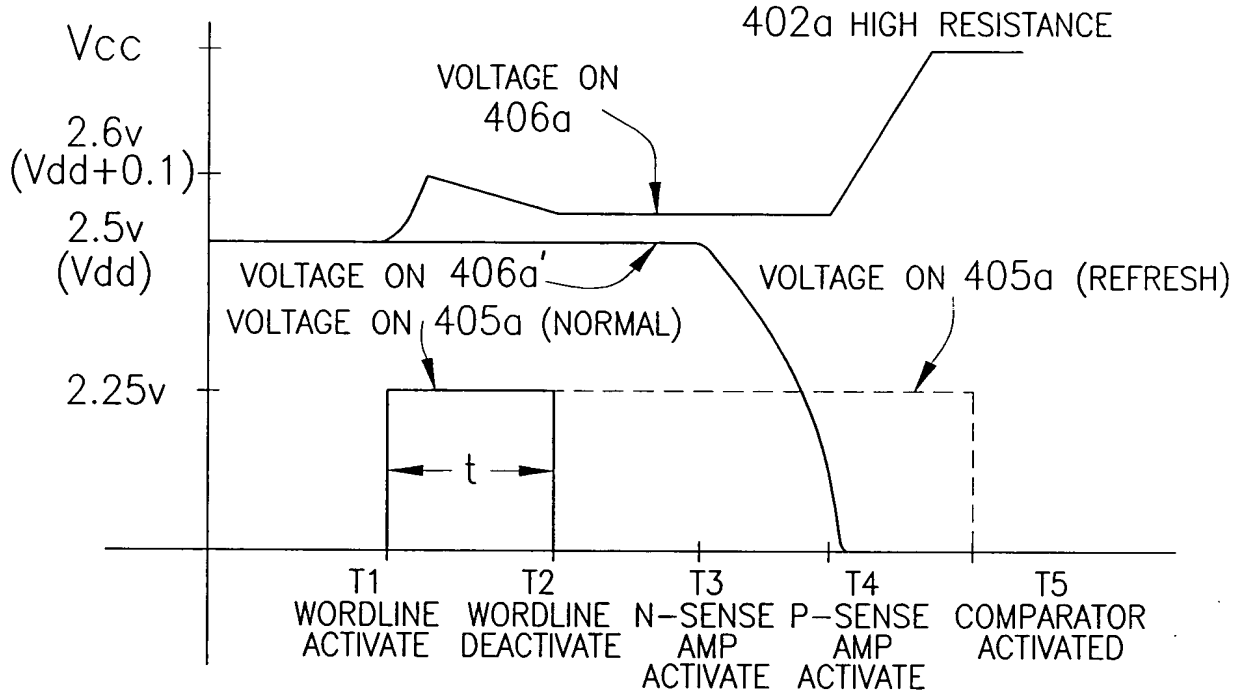

Vcc
2.6v
(Vdd+0.1)
2.5v
(Vdd)
2.25v
402a HIGH RESISTANCE
VOLTAGE ON 406a
VOLTAGE ON 406a'
VOLTAGE ON 405a (NORMAL)
VOLTAGE ON 405a (REFRESH)
t
T1 WORDLINE ACTIVATE
T2 WORDLINE DEACTIVATE
T3 N-SENSE AMP ACTIVATE
T4 P-SENSE AMP ACTIVATE
T5 COMPARATOR ACTIVATED

FIG. 6B

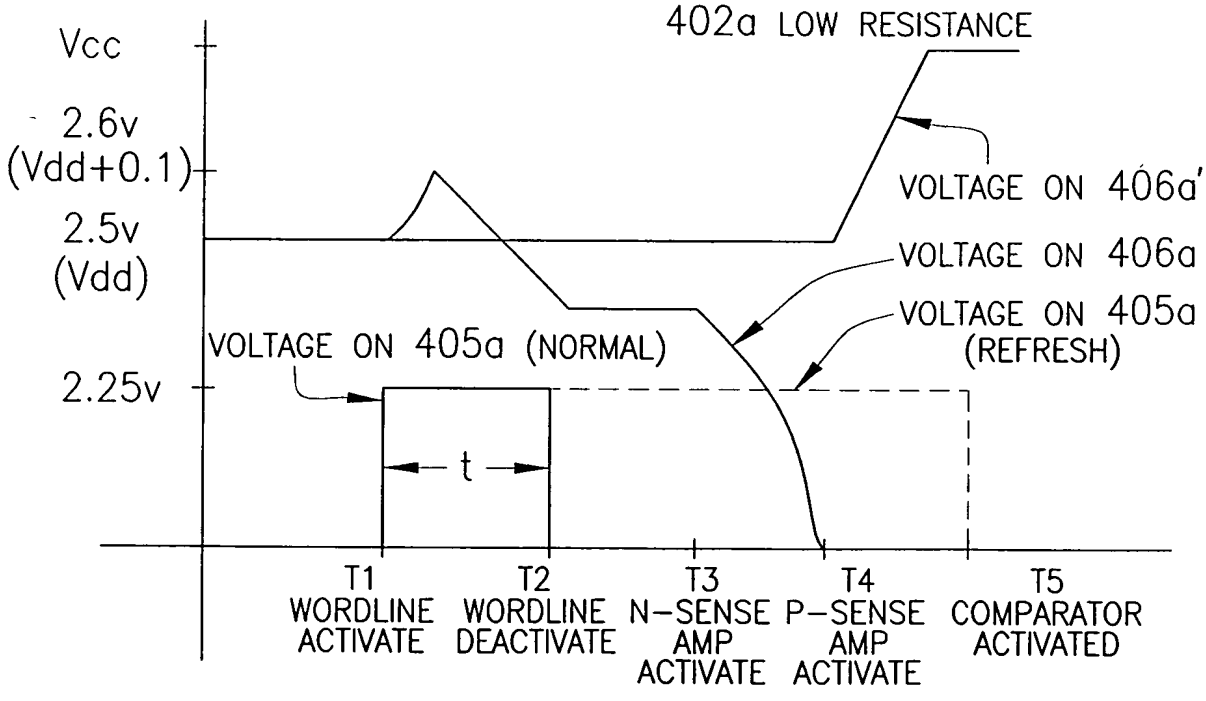

Vcc
2.6v
(Vdd+0.1)
2.5v
(Vdd)
2.25v
402a LOW RESISTANCE
VOLTAGE ON 406a'
VOLTAGE ON 406a
VOLTAGE ON 405a (REFRESH)
VOLTAGE ON 405a (NORMAL)
t
T1 WORDLINE ACTIVATE
T2 WORDLINE DEACTIVATE
T3 N-SENSE AMP ACTIVATE
T4 P-SENSE AMP ACTIVATE
T5 COMPARATOR ACTIVATED

FIG. 7

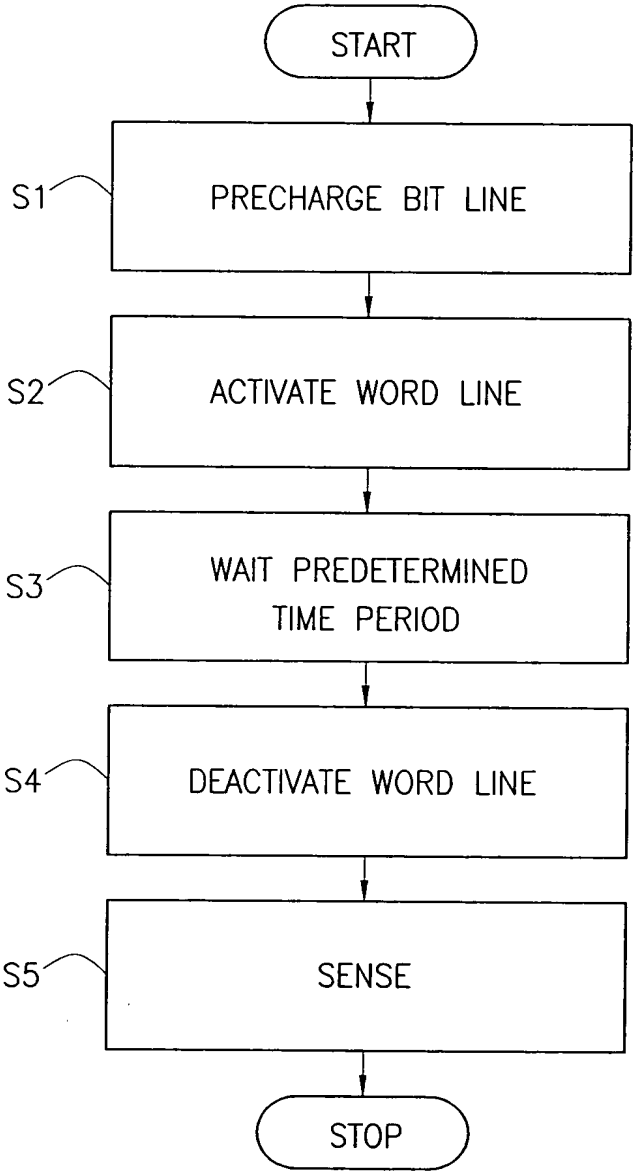

START
S1
PRECHARGE BIT LINE
S2
ACTIVATE WORD LINE
S3
WAIT PREDETERMINED TIME PERIOD
S4
DEACTIVATE WORD LINE
S5
SENSE
STOP

FIG. 8

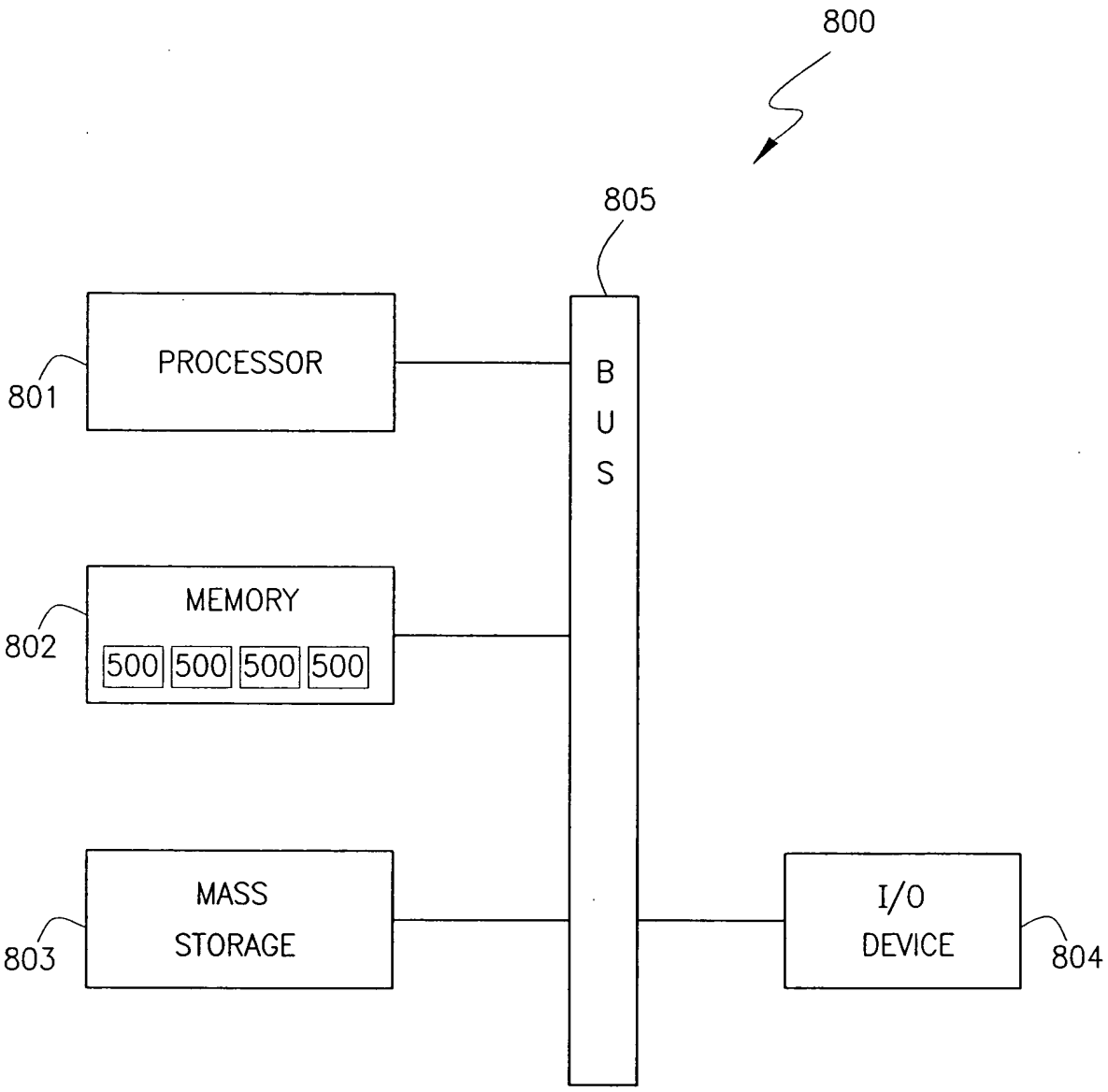
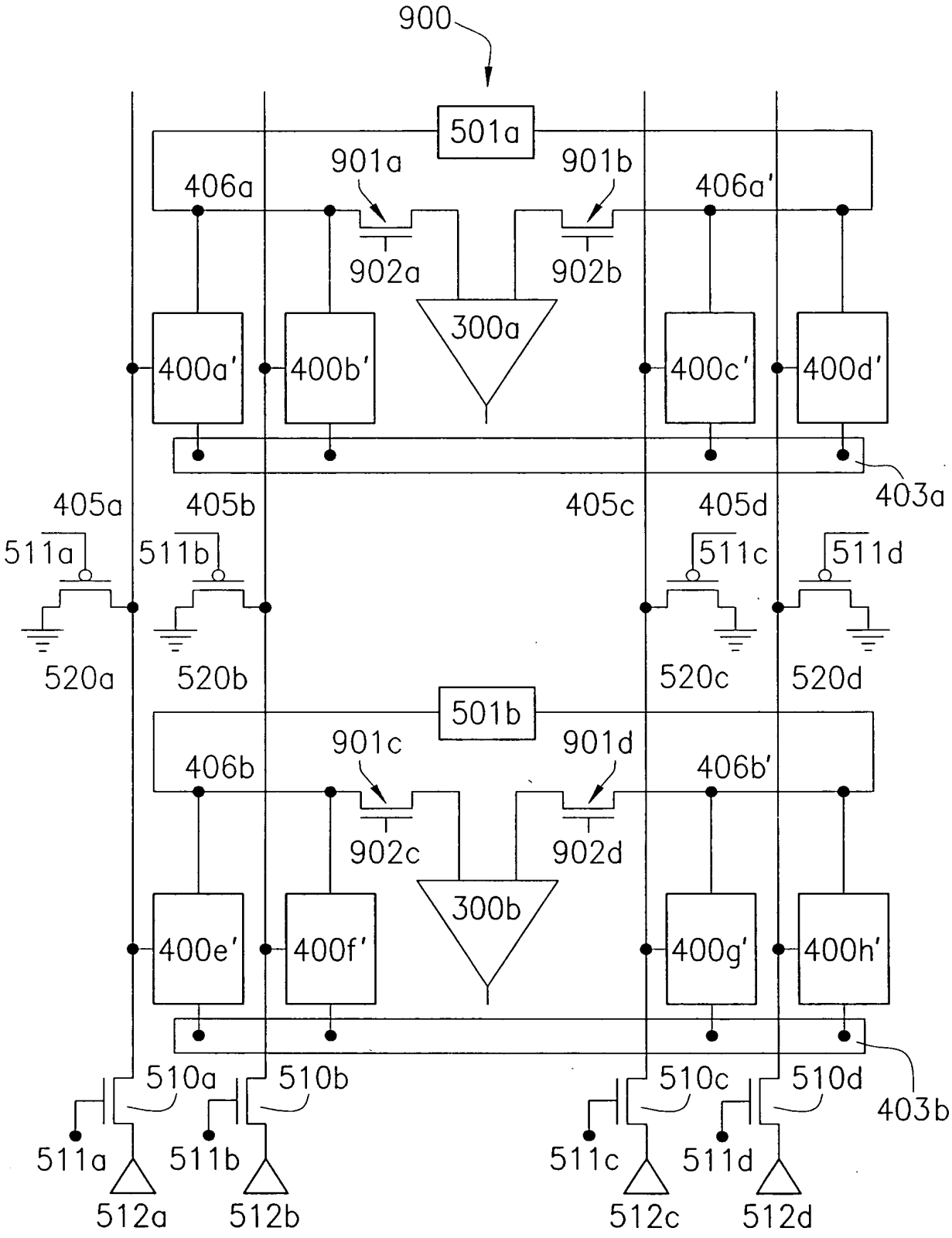

800
805
PROCESSOR
801
B
U
S
MEMORY
802
500
500
500
500
MASS
STORAGE
803
I/O
DEVICE
804

FIG. 9


900
501a
406a
901a
901b
406a'
902a
902b
300a
400a'
400b'
400c'
400d'
403a
405a
405b
405c
405d
511a
511b
511c
511d
520a
520b
520c
520d
501b
406b
901c
901d
406b'
902c
902d
300b
400e'
400f'
400g'
400h'
403b
510a
510b
510c
510d
511a
511b
511c
511d
512a
512b
512c
512d

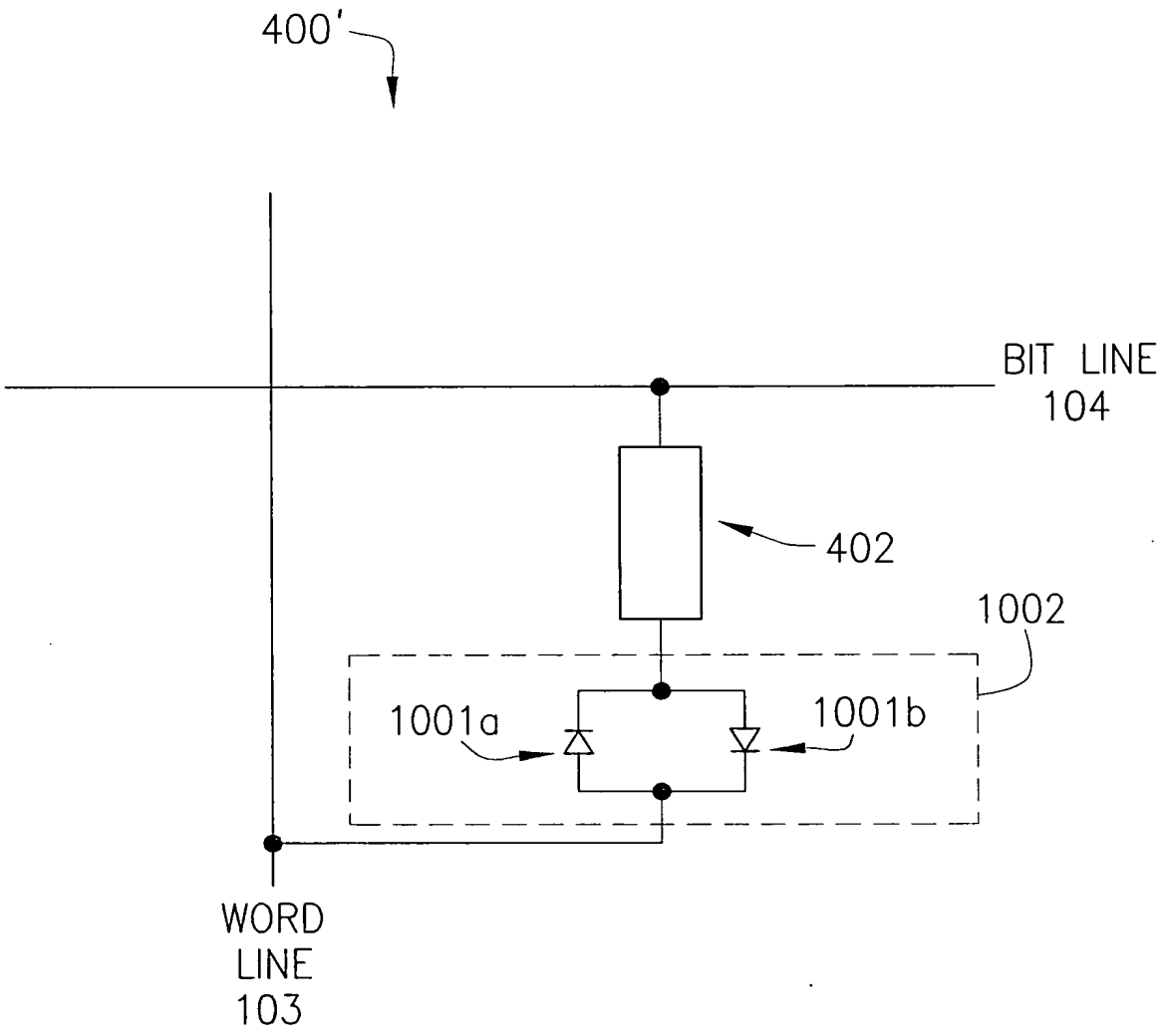



FIG. 10